

As of 06.08.2025

# AURIX™ TC4xx Crash Course: 32-Bit Multicore Microcontroller Family (Aurix-3G Third Generation) - Face-to-Face Training

#### **Objectives**

You know the architecture and particularly the innovations and features (multicore and safety extensions) of the latest generation of the AURIX™ device family.

You can efficiently adapt your software architectures to hardware, thus developing high-performance systems.

The compact training format enables you to quickly implement your new knowledge in your projects.

#### YOUR BENEFIT:

Efficient and compact jump-start into the overall topic (saves three months according to our customers)

Practical tips on multicore and safety

#### **Participants**

Integrators, architects, developers, test engineers, those switching to or starting to work with AURIX™

#### Requirements

Experience in microcontroller/microprocessor system programming and architecture. Knowledge of earlier AURIX generations is an advantage but not a requirement.

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#### Content

## Introduction

- History
- Markets and applications
- Key differentiators
- Main building blocks

#### **System Architecture**

- Block diagrams
- Clustering und accelerators
- Main CPU subsystems
- Memory architecture
- Buses
- Conclusions for software architecture

## Infrastructure

- Crossbars
- Peripheral buses
- Bridges

#### Virtualization

- Use cases
- Implementation patterns

#### TriCore™ CPU Subsystems

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- Core architecture
- Block diagram
- Pipelines
- Core specific function registers
- Register files and context switching
- Specific instructions and spinlock example
- Extensions for virtualization
- Trap system
- Memory protection unit (MPU)
- System timer (STM)

## **Protection Mechanisms**

- PROT
- Access protection unit (APU)

## Interrupt Router

- Configuration
- Software trigger
- Broadcasting
- External Interrupts

## **System Control and Management**

- Clocking
- Non maskable interrupts (NMI)
- Reset
- External service request pins (ESR)
- System modes
- Booting

## **Safety Concept**

- Measures
- Safety and security management unit (SMU)

## **Security Concept**

- Cybersecurity real-time module (CSRM)
- Cybersecurity satellite

## **Debug and Trace Aspects**

- New internal architecture
- SMP vs. AMP debug

#### **IMPORTANT NOTE:**

- A valid NDA with the chip vendor is a pre-requirement to attend the Aurix-3G crash course.

## **FACE-TO-FACE TRAINING**

Price \* Duration 1.875,00 € 2.5 days Training code: E-A3GCRSH

\* Price per attendee, in Euro plus VAT

## Live Online - English

#### **Duration**

2.5 days

#### Face-To-Face - German

## Duration

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## Coaching

Our coaching services offer a major advantage: our specialists introduce their expertise and experience directly in your solution process, thus contributing to the success of your projects.

We will be happy to provide you with further information or submit a quotation tailored to your requirements.