

## Armv8-R Workshop: 32-Bit Cortex® Microcontroller Core for Real-Time Applications in Automobiles, the Industry and Embedded Systems - Live Online Training

### Objectives

You know the architecture, features and advantages of the Armv8-R (real-time) core architecture.

You learn how to choose and make efficient use of the right microcontrollers with the respective cores.

You can write software in C and Assembler and utilize safety and security mechanisms - the perfect start for designing Cortex® v8-R based systems.

### YOUR BENEFIT:

Efficient and compact jump-start into the overall topic

Practical tips on multicore, safety and security

Download of exercises

Extensive training documentation helps you apply and reproduce what you learned.

### Participants

Hardware and software architects, hardware and software developers, test engineers

### Requirements

ANSI-C knowledge; experience in microcontroller/microprocessor system programming and architecture

### Live-Online-Training

17.03. – 20.03.2026 3.000,00 € 4 Days

\* Price per attendee, in Euro plus VAT

Training code: LE-ARMV8R

### Face-To-Face - English

**Date**                   **Duration**

10.11. – 13.11.2026 4 days

### Live Online - German

**Date**                   **Duration**

17.03. – 20.03.2026 4 days

### Face-To-Face - German

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### **Content**

**Overview Arm®v8 Real Time Profile**

**Cortex® R52 Processor Architecture**

#### **Instruction Sets**

**Synchronization and Barriers**

- Exclusive monitors

**Writing C for Arm**

**Exceptions and Handling**

- Exception levels
- Interrupts and aborts
- Interrupt controller architectures
- Routing and trapping
- Nesting and returning

#### **Timer**

- Generic timer
- Performance monitor unit

**Internal Connectivity and Memory**

- Bus interfaces
- Tightly coupled memory and caches
- Performance aspects

**Memory Protection Unit**

- Purpose and use cases
- Regions and attributes

**Safety Aspects**

- Register protection
- Indirect memory access
- Dual core lockstep
- ECC
- Error reporting

**Debug and Tracing**

**Virtualization**

- Use cases
- Hypervisor
- Temporal and spatial separation
- Identification
- Asynchronous stimuli

**Exercises**