MICRO CONSULT

Stand 01.05.2026

Cortex®-A5, A7, A8, A9, A15, A17: Arm® Cortex-A Architektur - Live-Online-Training

**Ziele -
Ihr Nutzen**

Sie kennen die Cortex®-A Architektur und können Programme in Assembler und C erstellen. Sie haben den perfekten Einstieg in die Entwicklung von Arm-basierenden Systemen.

Teilnehmer

Software- und Hardware-Entwickler. (Sollten Sie bereits das Training "Arm7/9/10/11: Architektur und Embedded Programmierung" besucht haben, setzen Sie sich bitte vorab mit uns in Verbindung).

Voraussetzungen

ANSI-C und Mikrocontroller-Grundkenntnisse.

Live Online Training

* Preis je Teilnehmer, in Euro zzgl. USt.

Anmeldecode: L-CORAX

Präsenz-Training - Deutsch

Dauer
4 Tage

Präsenz-Training - Englisch

Dauer
4 Tage

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Inhalt

Cortex®-Ax Processor Architecture

- Operating Modes, States, Pipeline, Register-Organization
- User Mode, Fast Interrupt (FIQ) Mode, Interrupt (IRQ) Mode
- Supervisor Mode, System Mode, Undefined Mode, Secure Monitor Mode
- Thumb-2 State, Arm State, Jazelle State, ThumbEE State
- Cortex®-Ax Register File
- Status Register

Arm Processor Cores: Overview

- Cortex®-M, Cortex®-R, Cortex®-A Processor Cores
- Arm7 / Arm9 / Arm10 / Arm11

Arm, Thumb-2 and DSP Instruction Sets

- v7 Thumb-2 Instruction Set
- Arm/Thumb Interworking
- Most important Assembler Directives
- v4, v4T, v5, v6 Instruction Set Overview

Advanced SIMD and VFP Extension

- NEON Coprocessor
- VFP Floating Point Unit

Jazelle RCT Extension Overview

- Thumb-2EE Instruction Set
- ThumbEE State

Exception Handling

- Exception Modes: FIQ, IRQ, ABORT, UNDEF, SVC, SMC
- Exception Handler Templates
- Vector Tables: Normal, Secure, Monitor Mode
- TrustZone (Secure) Exception Handling
- Exception Handling in Singlecore and Multicore Systems
- Global Interrupt Controller (GIC)
- Vector Interrupt Controller (VIC)
- Generic Interrupt Controller (GIC)

System Control Coprocessor, CP15

- Arm Coprocessor Concept, CP0 ... CP15
- Overall System Control & Configuration
- Cache Configuration and Cache Management
- Memory Management Unit (MMU) Configuration
- System Performance Monitoring (PMU)

Level 1 Memory System

- Instruction and Data Cache
- Cache Initialization
- Store Buffer

Level 2 Memory System

- Advanced Microprocessor Bus Architecture (AXI)
- AXI Bus Masters
- AXI Bus Slaves
- Second Level Caches
- Preload Engine (PLE)
- On-chip RAM and Flash, Peripherals
- External Memory Interface (EMI)

Memory Management Unit MMU

- Translation lookaside buffer (TLB)
- Translation and Page Tables, Attributes
- Virtual Addressing, Tablewalk

Cortex®-Ax Multiprocessor Core

- Primary, Secondary CPU
- Global Interrupt Controller (GIC)
- Snoop Control Unit (SCU)
- Accelerator Coherency Port (ACP)
- Address Filtering

Startup Singlecore System

- Startup File
- Vector Table, Stack, PLL and Data Initialization
- Cache, MMU and Branch Predictor Initialization
- From Reset to main

Startup Multicore System

- From Reset to main
- Primary CPU Initialization
- Secondary CPU Initialization

Clock, Reset and Power Control

- Low Power Modes

TrustZone Extension

- TrustZone Overview
- Secure Monitor Mode
- TrustZone Exception Handling
- Startup in Secure World
- Switch from Secure World to Non-secure World

Virtualization Extension

- Hyp Mode
- Hypervisor
- Large Address Extension
- L1 and L2 Tablewalk

Cortex®-Ax Debug Support

- Embedded Trace Macrocell (ETM)
- Program Trace Macrocell (PTM)
- CoreSight Debug Components
- Performance Monitoring Unit (PMU)
- Cross Trigger Unit (CTU)
- Debug Coprocessor, CP14

Software Development: Overview

- CMSIS for Cortex®-A
- Compiler Options
- Linker Options
- Linker Description File
- Locating Program and Data in Memory

Übungen zu den Themen mit der IAR Workbench und einem Evaluation Board