MicroConsult

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Cortex®-R4, R5, R7, R8: Arm® Cortex-R Architecture Training - Face-to-Face Training

Objectives

You know the Cortex® R4, R5, R7 and R8 architecture and can write software in C and Assembler. You can place the programs in memory and test them. You get the perfect introduction in developing Cortexbased systems.

Participants

Software and hardware developers. If you already attended our Training "Arm7/9/10/11: Architecture and Embedded Programming", please contact us prior to booking.

Requirements

A basic understanding of ANSI-C and microcontrollers.

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Content

Arm Cortex Processor Architecture

- Register organization, operation modes, states, pipeline

Arm Processor Cores - Overview

- Cortex®-R4, -R5, -R7, -R8 processor core
- Cortex®-Av7, Cortex™-Av8 processor cores
- Cortex®-Mv7, Cortex®-Mv8 processor cores
- Arm7/9/11 processor core

Arm, Thumb, Thumb-2 Instruction Sets

- Arm v4, v4T, v5, v6 instruction set
- Thumb instruction set
- v7 Thumb-2 instruction set
- Data barriers, instruction barriers
- Synchronization, load/store exclusice instructions
- ARM/Thumb interworking
- Assembler directives

Exception Handling

- FIQ, IRQ, abort, supervisor call, undefined
- Exception handler examples
- Vectored interrupt controller, VIC
- Generic interrupt controller, GIC

Coprocessors, Floating Point Unit

- Arm coprocessor concept
- System controller CP15
- Floating point unit, FPU
- System configuration

L1 Memory Interface

- Tightly coupled memory, cache architecture
- Memory protection unit, MPU

L2 Memory Interface

- Advanced microprocessor bus architecture - AXI

- Master interface
- Slave interface

Debug, Trace, Performance Monitoring

- Watchpoint units, embedded trace macrocell ETM
- Performance monitor unit, PMU

Multi-Processing Features

- Private memory region
- Snoop control unit, SCU
- Hardware coherency management
- Split mode (performance mode)
- Locked mode (safety mode)

Power Modes

- Run, standby, dormant, shutdown

Embedded Software Development

- Adjustment of library routines to hardware (retargeting)
- Placing code and data in memory (scatter loading)
- Linker description file
- Reset, start-up, start-up file
- From reset to main

Efficient C programming for Cortex architectures

- Compiler optimization, compiler options
- Interface C - Assembler
- Programming guidelines for Arm compilers
- Optimized utilization of local and global data

Hardware-near C

- C statements and their execution in Assembler
- Access to peripherals in C
- Layer model for embedded systems
- Structured description of peripherals

Practical Exercises with Keil µVision and Arm RealView Tools

- Different tools can be used on request
- All programs are tested on an evaluation board

FACE-TO-FACE TRAINING

Price *	Duration
-	4 days

Training code: E-CORRX
* Price per attendee, in Euro plus VAT

Face-To-Face - German

Duration

4 days

Live Online - German

Duration

4 days

Coaching

Our coaching services offer a major advantage: our specialists introduce their expertise and experience directly in your solution process, thus contributing to the success of your projects.

We will be happy to provide you with further information or submit a quotation tailored to your requirements.

More trainings on www.microconsult.com. Subject to change.
All prices per attendee, in EUR plus VAT.
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