As of 18.02.2026

AURIX™ TC2xx Workshop: 32-Bit Multicore Microcontroller Family - Face-to-Face Training

Objectives

You know the architecture, basic on-chip peripherals and features (especially of the multicore architecture and safety extensions) of the AURIX™ device family.

You are able to program low-level drivers for this hardware, adapt them and test them with a debugger.

You can moreover generate interrupt and trap routines.

YOUR BENEFIT:

Efficient and compact jump-start into the overall topic

Practical tips on multicore and safety

Tips on how to create an efficient software architecture

Download of exercises

Participants

Hardware and software architects, hardware and software developers, test engineers // IMPORTANT NOTE: A valid NDA with the chip vendor is a pre-requirement to attend the course.

Requirements

ANSI-C knowledge; experience in microcontroller/microprocessor system programming and architecture

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Content

Infineon AURIX™ Architecture: Overview

AURIX™ Multicore

- CPU, pipelines, register sets, floating point unit FPU, DSP extension
- Memory model, local and global memory units
- On-chip bus systems: 64-bit XBAR, 32-bit system peripheral bus SPB
- TRAP handling

Ports (Pin Definition and Port Functions)

Protection System

Multicore Interrupt Processing: Interrupt Router

Direct Memory Access Controller DMA

On-Chip AURIX™ Peripherals

Timer

- System timer module STM
- Generic timer module GTM
- Capture and compare unit CCU6

Communication Interfaces

- UART/LIN, QSPI, I2C, MSC, HSSL & HSCT
- Overview: MultiCAN, Ethernet, FlexRay®

Sensor Interfaces

- Single edge nibble transmission SENT
- Peripheral sensor interface PSI5

Analog-to-Digital Converter

- Versatile analog-digital converter VADC
- Delta-sigma analog-digital converter DSADC

System Control Unit SCU

- Clock control
- Reset system
- Power management
- External request unit ERU
- Start-up process
- Watchdog timer WDT

Safety

On-chip Debug System OCDS

Overview: Emulation Device & Calibration

Exercises

- Exercises are performed with an Infneon AURIX™ board, covering the following aspects: interrupt controller, DMA controller, multicore start-up, initialization of peripherals.
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IMPORTANT NOTE: A valid NDA with the chip vendor is a pre-requirement to attend the course.

ADAS specific blocks are not covered

FACE-TO-FACE TRAINING

Price *	Duration
-	5 days

Training code: E-AURIX
* Price per attendee, in Euro plus VAT

Live Online - English

Duration
5 days

Face-To-Face - German

Duration
5 days

Live Online - German

Duration
5 days

Coaching

Our coaching services offer a major advantage: our specialists introduce their expertise and experience directly in your solution process, thus contributing to the success of your projects.

We will be happy to provide you with further information or submit a quotation tailored to your requirements.

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