Stand 28.03.2024

AURIX™ TC2xx Workshop: 32-Bit Multicore Microcontroller Family - Face-to-Face Training

**Ziele -
Ihr Nutzen**

You know the architecture, basic on-chip peripherals and features (especially of the multicore architecture and safety extensions) of the AURIX™ device family.

You are able to program low-level drivers for this hardware, adapt them and test them with a debugger.

You can moreover generate interrupt and trap routines.

YOUR BENEFIT:

Efficient and compact jump-start into the overall topic

Practical tips on multicore and safety

Tips on how to create an efficient software architecture

Exercises on USB stick or as download.

Teilnehmer

Hardware and software architects, hardware and software developers, test engineers // IMPORTANT NOTE: A valid NDA with the chip vendor is a pre-requirement to attend the course.

Voraussetzungen

ANSI-C knowledge; experience in microcontroller/microprocessor system programming and architecture

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Inhalt

Infineon AURIX™Architecture: Overview

AURIX™ Multicore

- CPU, pipelines, register sets, floating point unit FPU, DSP extension
- Memory model, local and global memory units
- On-chip bus systems: 64-bit XBAR, 32-bit system peripheral bus SPB
- TRAP handling

Ports (Pin Definition and Port Functions)

Protection System

Multicore Interrupt Processing: Interrupt Router

Direct Memory Access Controller DMA

On-Chip AURIX™ Peripherals

Timer

- System timer module STM
- Generic timer module GTM
- Capture and compare unit CCU6

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Alle Preise sind Nettopreise pro Person zzgl. gesetzlicher USt.
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Communication Interfaces
- UART/LIN, QSPI, I2C, MSC, HSSL & HSCT
- Overview: MultiCAN, Ethernet, FlexRay®

Sensor Interfaces
- Single edge nibble transmission SENT
- Peripheral sensor interface PSI5

Analog-to-Digital Converter
- Versatile analog-digital converter VADC
- Delta-sigma analog-digital converter DSADC

System Control Unit SCU
- Clock control
- Reset system
- Power management
- External request unit ERU
- Start-up process
- Watchdog timer WDT

Safety

On-chip Debug System OCDS

Overview: Emulation Device & Calibration

Exercises
- Exercises are performed with an Infneon AURIX™ board, covering the following aspects: interrupt controller, DMA controller, multicore start-up, initialization of peripherals.
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ADAS specific blocks are not covered

Präsenz-Training

Termin	Preis *	Dauer
15.07.2024 – 19.07.2024	3.500,00 €	5 Tage

* Preis je Teilnehmer, in Euro zzgl. USt.

Anmeldecode: E-AURIX

Live-Online - Englisch

Dauer
5 Tage

Präsenz-Training - Deutsch

Termin	Dauer
15.07. – 19.07.2024	5 Tage

Live-Online - Deutsch

Dauer
5 Tage

Coaching

Unsere Coaching-Angebote bieten den großen Vorteil, dass unsere Experten ihr Wissen und ihre Erfahrungen

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direkt in Ihren Lösungsprozess einbringen und damit unmittelbar zu Ihrem Projekterfolg beitragen.

Für Ihre Anfrage oder weiterführende Informationen stehen wir Ihnen gern zur Verfügung.

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